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TDB-ACC-NO: NB8908403

DISCLOSURE TITLE: Single-Crystal Silicon Embedded With Insulated Conducting Wires

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, August 1989, US

VOLUME NUMBER: 32

ISSUE NUMBER: 3B

PAGE NUMBER: 403 - 407

PUBLICATION-DATE: August 1, 1989 (19890801)

CROSS REFERENCE: 0018-8689-32-3B-403

DISCLOSURE TEXT:

- In packaging technology, a generic problem is that the packaging materials tend to have a different thermal expansion coefficient from that of silicon. Consequently, upon thermal cycling during operation a shear stress is exerted on those solder balls that join the chip and module, and fatigue failure of the balls occurs.

This problem limits the size of the chip since the magnitude of the shear depends on the chip size. In order to overcome this problem so that a large chip can be used in VLSI, there has been a long term effort to develop ceramics which have the same thermal

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2	JP 2001144150		JPO	20010525	9	WAF
3	JP 10162613 A		JPO	19980619	8	LIG
4	JP 09237826 A		JPO	19970909	8	ELE
5	JP 01179353 A		JPO	19890717	4	MAN
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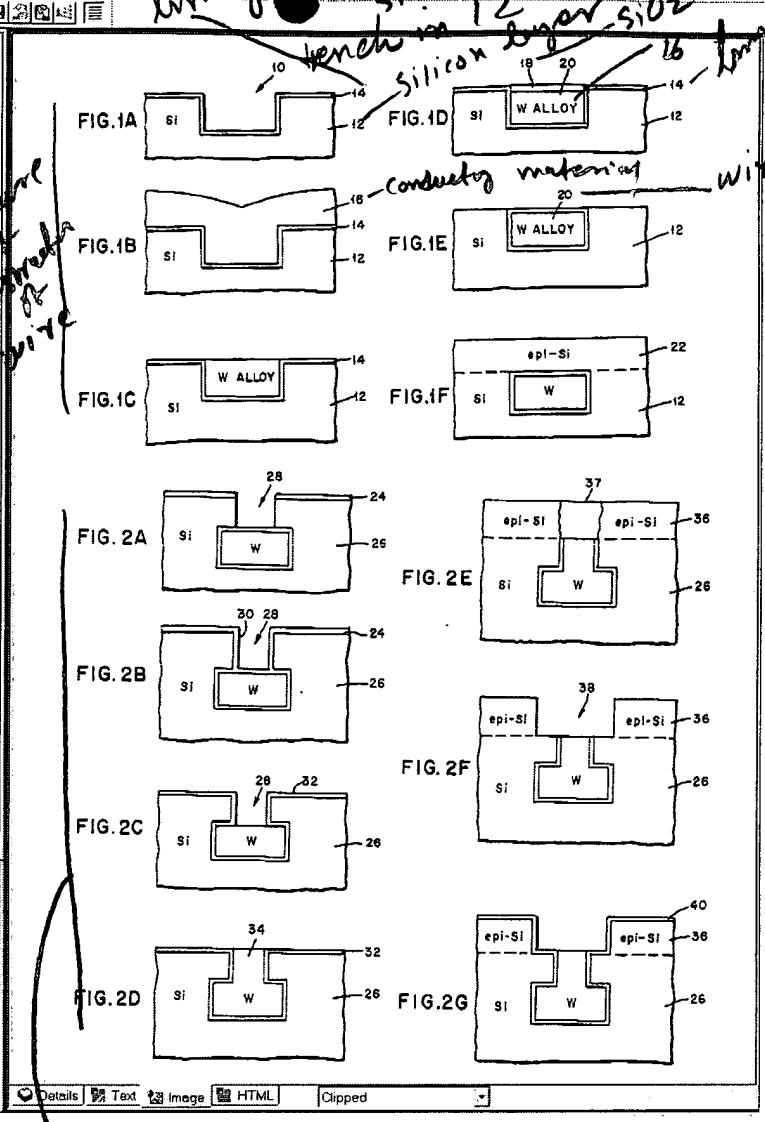

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Page 7

TDB-ACC-NO: NB8908403

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This problem limits the size of the chip since the magnitude of the shear depends on the chip size. In order to overcome this problem so that a large chip can be used in VLSI, there has been a long term effort to develop ceramics which have the same thermal expansion coefficient as that of silicon. However, the material which has the best match of expansion coefficient with silicon is silicon itself.

- In order to use silicon as a packaging material, it must be

possible to lay conducting wires and vias within it, same as with the multi-layered ceramic (MLC) substrates used today. To achieve this, a method is described to construct a three-dimensional network of insulated conducting lines within a single-crystal silicon. The procedure for the construction of a wire is illustrated in Figs. 1A - 1F, and of a via in Figs. 2A - 2G. ***** SEE ORIGINAL DOCUMENT *****

Wire Construction

A line trench 10 is first etched in silicon layer 12. Fig. 1A shows the trench 10 (the cross-section of a line) having a lining 14 comprised of SiO2/Si3N4/SiO2.

Fig. 1B shows the conformal deposition of a conducting material 16, such as W containing about 5 at .% of Si, or WSi2 containing about 5 at .% excess Si.

Fig. 1C shows planarization of the surface by chemical and mechanical polishing and etching away the excess W alloy or silicide.

Fig. 1D shows oxidation of the W alloy or silicide to produce a thick layer 18 of SiO2 on top of the line 20. Because SiO2 is thermodynamically more stable than the oxides of W, it will form on the surface of the line. The composition of Si in the W alloy or silicide line 20 is chosen so that a thick SiO2 layer 18 can grow on the wire surface.

Fig. 1E shows that by chemical etching, the oxide and nitride on the Si surface are removed. Because the oxide 18 on the line is thick, a layer of SiO2 will survive the etching and insulate wire 20.

Fig. 1F shows that by epi-Si and SOI (Si on Insulator) growth, a Si layer 22 can be grown on the wire in a single

crystal Si environment.

- This procedure can be repeated to produce a second layer of wires. Nevertheless, vias or through-holes are needed between them for interconnection.

- Via Construction: Fig. 2A shows the growth or deposit of a thick thermal SiO2 layer 24 on the surface of Si layer 26. By lithographic patterning, via hole 28 is opened in the oxide by etching, after which reactive ion etching is used to drill a via in the Si 26. Drilling stops at the bottom oxide surface of the via.

Fig. 2B shows the growth of a sidewall oxide 30 on the via. Some oxide growth will occur simultaneously on the surface as well as on the bottom via surface. Fig. 2C shows that by reactive ion etching (RIE) the oxide on the bottom surface of the via can be removed. This etching will remove an equal thickness of the oxide on the top surface. Since it is thicker, a layer 32 of oxide remains on the top surface after etching. Due to the directional effect of RIE, the sidewall oxide of the via will not be etched away. In Fig. 2D, the via is filled by selective deposition of W (or WSi2), i.e., the W grows only on the W (or WSi2) surface but not on the SiO2 surface, resulting in a via surface 34 that is planar with its surrounding. In Fig. 2E, the oxide on the Si surface is etched away and an epi-Si layer 36 is grown over Si layer 26. At the same time, silicide and poly-Si region 37 will grow over the via. The epi- Si has a thickness the same as the wire thickness.

- Fig. 2F shows that when a line trench 38 is

etched over the via, the silicide and poly-Si 37 over the via are removed. The poly-Si can be etched selectively to form an extended via hole by using an etchant which attacks epi-Si and poly-Si at different rates. Fig. 2G shows that a lining 40 of SiO2/Si3N4/iO2 is formed on the second trench. Laser etching or RIE is used to remove the very thin oxide just over the via before filling the second level trench with W alloy or silicide again. W or WSi2 can be used as conducting materials in this process.

Other conductors also can be used, but they must have a melting point higher than the processing temperatures involved. For example, Al is not good since its melting point is lower than that (1050oC) used to grow epi-Si. Also, the conductor must be stable with SiO2 which is the isolating material used here. For example, Ti is not a good choice since it decomposes SiO2 upon annealing above 400oC. For the same reason, when a Ti-Si alloy is oxidized, it is the oxide of Ti rather than SiO2 that will form preferentially on the surface. Therefore, only certain transition metals, such as W, Mo, Pt, Co, etc., can be used. Transition metal silicides and noble metals, such as Au and Cu containing a few percent of excess Si, are generally suitable.

Thermal stress in the line upon heating and cooling must be addressed. From this viewpoint, the best conducting line in Si is made of heavily doped poly-Si, provided that its conductivity is good enough for general purpose application. The stress problem is handled

by adding a few percent of Si into the metal conductor, such as W.

The Si is needed to form SiO2 on the line surface for isolation.

- When Si atoms diffuse to the surface to form an oxide,

vacancies diffuse back into the metal (or silicide) to form voids.

These voids will cushion the stress in the line, in particular the

compression stress which is more serious since it may crack the oxide

coating. Another technique to reduce the stress effect is to unfill

a small part of the trench during deposition by making use of the

shadow of the trench wall. The unfilled part again provides a

cushion space for stress relief.

- In planarizing the via, selective W deposition has been used.

It is a simple and available technique. On the other hand, this

technique has not been developed for other metals. Nevertheless, in

filling a via the procedure of filling a trench, as has been

disclosed here, can be followed.

- An important question about high density packing of conducting lines is how to achieve effective heat dissipation. Since cooling of a chip is necessary, one side of a Si wafer can be used to build active devices and the other side (the back side) of the wafer can be used for packaging purposes. In fact, wafers can be stacked one

on top of the other and joined by solder joints. For packaging

purposes, the quality of the epitaxial Si layer is not as critical as

that in the active side. In other words, some polycrystalline Si

grains in the epi-Si layer are tolerable.

- In device applications, for example, in a multi-layer SOI

technology, a random-access memory chip can be built in such a way that peripheral circuits are located over the cell array to save the chip area (*). In such applications both vertical and horizontal wires in between two silicon layers are needed for interconnections. The method disclosed here for making insulated wires in single-crystal Si is useful in multi-layer SOI technology.

Reference: * C. L. Cohen, "LSI in 3-D Coming Soon," Electronics Week, 16-17 (April 8, 1985).

EAST Browser - L2: (9) 1 and nitride | JP 02082641 A | Tag: S.P.T1 | Doc: 4/9 | "Full" 3/3 (Total images 3) | Marked

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PURPOSE: To improve mass productivity and reliability by forming a conductive path composed of the simple substance or complex of an interstitial nitride into a ceramic substrate obtained by sintering aluminum nitride and onto the surface of a sintered body.

CONSTITUTION: TiN paste in which polyvinyl butyral as a binding agent and isopropyl alcohol as a solvent are added to titanium nitride (TiN) is prepared. The molded form 5 of aluminum nitride (AlN) is formed, and conductive paths 2a, 2b are printed onto the surface of the molded form 5 by the TiN paste and dried. A molded form 6 in which Y<SB>2</SB>O<SB>3</SB> is added to AlN as a sintering assistant is shaped, and a plurality of conductive holes 6a are worked and the molded form 6 is superposed. Conductive paths 3a, 3b are printed by using the TiN paste, and dried. The whole is compressed in the thickness direction and unified, degreasing treatment is executed, and the whole is baked in a nitrogen atmosphere, thus acquiring a substrate, which is bonded firmly with a ceramic substrate, has the conductive paths having excellent oxidation resistance and has superior mass productivity and high reliability.

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2	JP 04233187 A		JPO	19920821	1	CER
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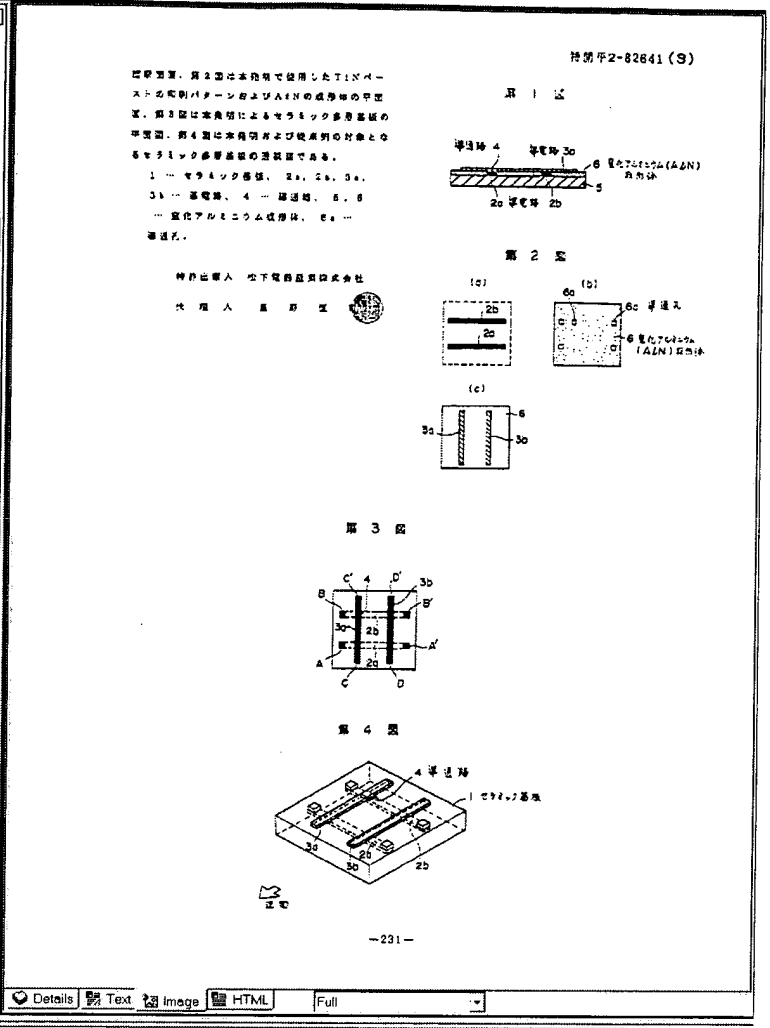

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ABSTRACT:

PURPOSE: To improve mass-productivity, realize complete coupling with a sintered Si<SB>3</SB>N<SB>4</SB> board and improve reliability by a method wherein layers of mixture of AlN, zirconium oxide and organic material and layers of mixture of AlN and organic material are alternately printed a plurality of times on the sintered Si<SB>3</SB>N<SB>4</SB> board and baked.

CONSTITUTION: Layers of insulator material and layers of material converted into conductor by the reaction at the time of baking are alternately printed a plurality of times on a sintered silicon nitride ceramic board 7 and baked. The insulator material printed on the surface of the ceramic board is composed of mixture of aluminum nitride and organic material. The material converted into conductor by the reaction at the time of baking is composed of a mixture of aluminum nitride, zirconium oxide and organic material. When the mixing ratio of aluminum nitride and zirconium oxide in the mixture of aluminum nitride, zirconium oxide and organic material is expressed by (AlN)<SB>x</SB>(ZrO<SB>2</SB>)<SB>1-x</SB>, zirconium nitride enough to provide a conductivity is made of the mixture having the composition (x)=0.2-0.9.

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6	JP 01230295 A		JPO	19890913		MAN
7	JP 01230294 A		JPO	19890913		MAN

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導電剤を構成する物質は焼成と同時に生成しており，前1ペースト入層および第2ペースト入層10との結合性も充分で，剥離に一体化していた。また，この導電層12a，12b，13aおよび13bを構成する物質はセラミックスであるため，耐久性が高く，耐酸化性においても酸素中で600℃，8時間の熱処理を行っても酸化は認められなかった。

なお，本実施例では，2種類のペースト入および8を得るための混合剤としてポリビニルブチラールを用いたが，他の樹脂を用いてもよく，また，溶媒にイソプロピルアルコールを用いたが，他の溶媒を用いてもよい。

また，AlNの焼結助剤として酸化イットリウムを添加したが，他の有効な焼結助剤を加えても，または加えなくても本発明が可能であることには変わりない。

一方，導電剤12a，12b，13aおよび13bを構成する物質が生成するAlNとZrO2の加工反応は，モル比でAlN：ZrO2＝3：1で起こる，従って，AlN：ZrO2＝3：1の組成で配合した混合物を窒素に対しているのが最も有効であるが，(AlN)x(ZrO2)1-xで表わした時にx＝0.2～0.9の組成の混合物で導電性を有するのに十分な酸化ジルコニウムが生成する。例えば，x＝0.3では酸化ジルコニウムの析成比率は約23重量％である。しかし，x＞0.9では酸化ジルコニウムの生成量が十分でなく，十分な導電性を得にくい。

〔発明の効果〕

以上説明したように，本発明によれば，Si3N4の焼結したセラミック基板の表面に，AlNと有機物質の混合物の列と，AlNとZrO2と有機物質の混合物の層を交互に複数印刷した後，焼成することにより，絶縁層の構成と導電層の形成が同時に行われるため，印刷時に位置を合わせる必要がなくなり，量産性が著しく向上する。また，形成される導電層はセラミックスであり，導電層と絶縁層であるAlNの焼結が同時に行われるため，両者の結合力は強固なものとなる。従って，セラミックスの導電層を有する耐久性，耐候性が大きく，高信頼性のセラミック多層基板が得られる。

4．図面の簡単な説明

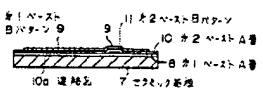
第1図は本発明によるセラミック多層基板の断面図，第2図は本発明によるセラミック多層基板における層の印刷パターンを示す平面図，第3図は本発明の一実施例によるセラミック多層基板の導電剤を示す平面図，第4図は従来の製造方法によるセラミック多層基板の断面図である。

1，7…セラミック基板，2…第1層，2a…空隙，3，8，12a，12b，13a，13b…導電剤，4…感光剤，5…第2層，6…第1ペースト入層，9…第1ペーストBパターン，10…第2ペースト入層，10a…導電孔，11…第2ペーストBパターン。

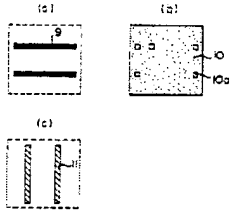
特許出願人　松下電器産業株式会社

代理人　萬　野　信

第1図



第2図



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US-CL-CURRENT: 264/680,427/96 ,428/901

ABSTRACT:

PURPOSE: To improve mass productivity, and obtain high reliability, by performing baking after a plurality of layers of material turning to conductor by reaction at the time of baking, and a plurality of layers of material being insulator are alternately printed on a sintered body of silicon nitride .

CONSTITUTION: On a sintered body 11 of silicon nitride, paste A12 is screen-printed on the whole surface, and dried at 150°C. After drying, thereon, paste B13 is screen-printed in a pattern as shown by (a), and dried in the same manner, After drying, thereon, paste A14 is screen-printed in a pattern as shown by (b), and dried in the same manner. After drying, thereon, paste B15 is printed in a pattern as shown by (c), and dried in the same manner. After this laminated body is degreased, baking is performed at 1800°C for two hours in a nitrogen atmosphere. The silicon nitride ceramic multilayer board obtained in this manner has a perfectly high conductivity in the printed part of paste B after baking. Since the material constituting a conducting channel is ceramics, the durability is high, and the oxidation resistance is large.

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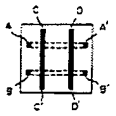
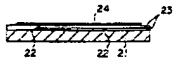
第 3 図



第 4 図



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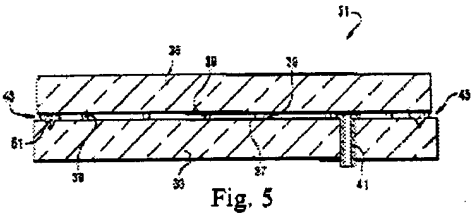

Fig. 5

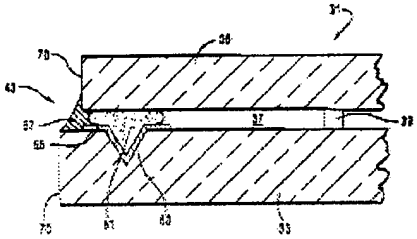

Fig. 6

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first glass substrate 33, second glass substrate 35, low pressure or evacuated space 37 between substrates 33 and 35, pillars 39 for spacing the substrates 33, 35 from one another and supporting them, optional pump out tube 41 disposed in a hole or aperture formed in substrate 33 for evacuating space 37, and peripheral or edge seal 43, 51 that hermetically seals low pressure space or cavity 37 between substrates 33, 35. Hermetic edge seal 51 prevents air from entering space 37 and keeps the vacuum therein. Seal 43, 51 is located in approximately the same peripheral location as seal 4 shown in FIG. 2. Reference numerals 43 and/or 51 may be used herein to refer to this peripheral or edge seal.

(6) IG units 31 according to different embodiments of this invention may be used as residential or commercial windows. The evacuation of space 37 eliminates heat transport between glass substrates 33 and 35 due to gaseous conduction and convection. In addition,

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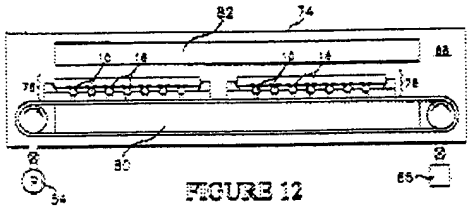

FIGURE 12

FIGURE 13A

FIGURE 15A

FIGURE 13B

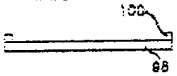

FIGURE 15B

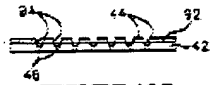

FIGURE 13C

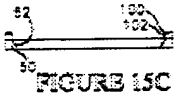

FIGURE 15C

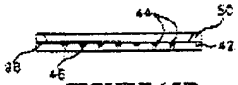

FIGURE 13D

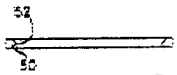

FIGURE 15D

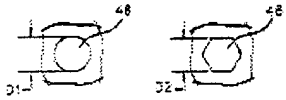

FIGURE 14A FIGURE 14B

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suitable wet etchant comprises HF. In addition, photosensitive glasses and etchants are commercially available from Dow Corning under the trademark "FOTOFORM".

(35) The diameter D2 (FIG. 5A) and depth D (FIG. 5A) of the ball retaining cavities 44 will be dependent on the size of etch openings 94 in the etch mask 92 and on the etch parameters. At the same time that the ball retaining cavities 44 are etched, the previously machined vacuum conduits 46 can also be etched. As shown in FIG. 14A, vacuum conduits 46 formed by laser machining will initially be circular in cross section. As shown in FIG. 14B, following an anisotropic wet etch with a silicon wafer blank 90, the vacuum conduits will have a multi faceted cross section (e.g., six sided).

(36) Following the etch procedure, the etch mask 92 can be stripped using a suitable wet chemical. For an etch mask 92 comprising Si.sub.3 N.sub.4 one suitable wet chemical for stripping the mask 92 comprises H.sub.3 PO.sub.4.

(37) Next, as shown in FIG. 13D, the substrate alignment member 50 can be attached to the ball retaining plate 42. One method of attachment is by forming an adhesive layer 96 out of silicone

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Eric J. Jakola, both of Kanata, all of (CA)

ignee: Nortel Networks Limited, St. Laurent (CA)

ice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

pl. No.: 09/739,896

d: Dec. 20, 2000

. Cl.[7] H01R 12/00

. Cl. 439/70; 439/331

ld of Search 439/68, 70, 71, 439/330, 331

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U.S. PATENT DOCUMENTS

6,353,235 A 3/2000 Ikeya

6,075,255 A 6/2000 Liao et al.

,969 A * 12/1977 Dean

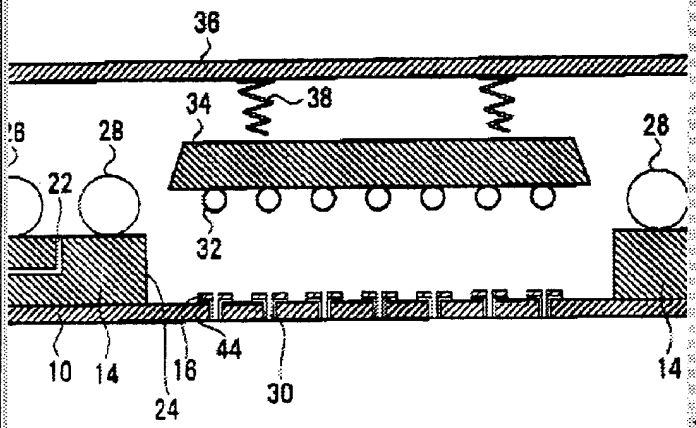
* cited by examiner

Primary Examiner—Khiem Nguyen

(57) **ABSTRACT**

The present invention relates to a socket in particular, high speed ICs in BGA pac of holding an IC package in the test soci resilient conductive test pads positioned array to match an array of spherical con of a BGA package. The BGA package is pads by the use of holes centered on the the spherical contacts are seated. The tes with two flexible seals on the top of encircle the test pads. The flexible seals, surface of a support and a socket lid, cavity to which a vacuum is applied. T thereby compressed pulling the socket ing the IC package leads into contact w

25 Claims, 2 Drawing S



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L14: (20) 13 AND (439/... | US 6416332 B1 | Tag: S | Doc: 4/20 | F...

square opening 24 defined in it.
The opening 24 surrounds a plurality of conductive test pads 16 on the top surface of the substrate 10. The conductive test pads 16 are comprised of a resilient conductive material which will deform when subject to compressive force and then return to its former shape when the compressive force is removed. An example of such a material is an electrically conductive elastomer which may be screen printed onto the surface of the substrate 10 prior to assembly of the support 14 to the substrate 10 and is typically in the range of 0.25 millimeters to 0.50 millimeters in thickness. Other possible materials include polycarbonates and conductive thermoplastic compounds. Preferably, the material from which conductive test pads 16 are constructed may be removed and replaced when it is damaged avoiding the need to replace the entire substrate 10. The conductive test pads 16 depicted in FIG. 1 are circular in shape however, other geometries of conductive test pads 16, such as square shaped pads, may be used.

(7) The conductive test pads 16 have holes 30 through their centers, preferably extending through both conductive test pads 16 and substrate 10. The holes 30 may or may not be conductively plated within the substrate 10. Between the conductive test pads 16 and the

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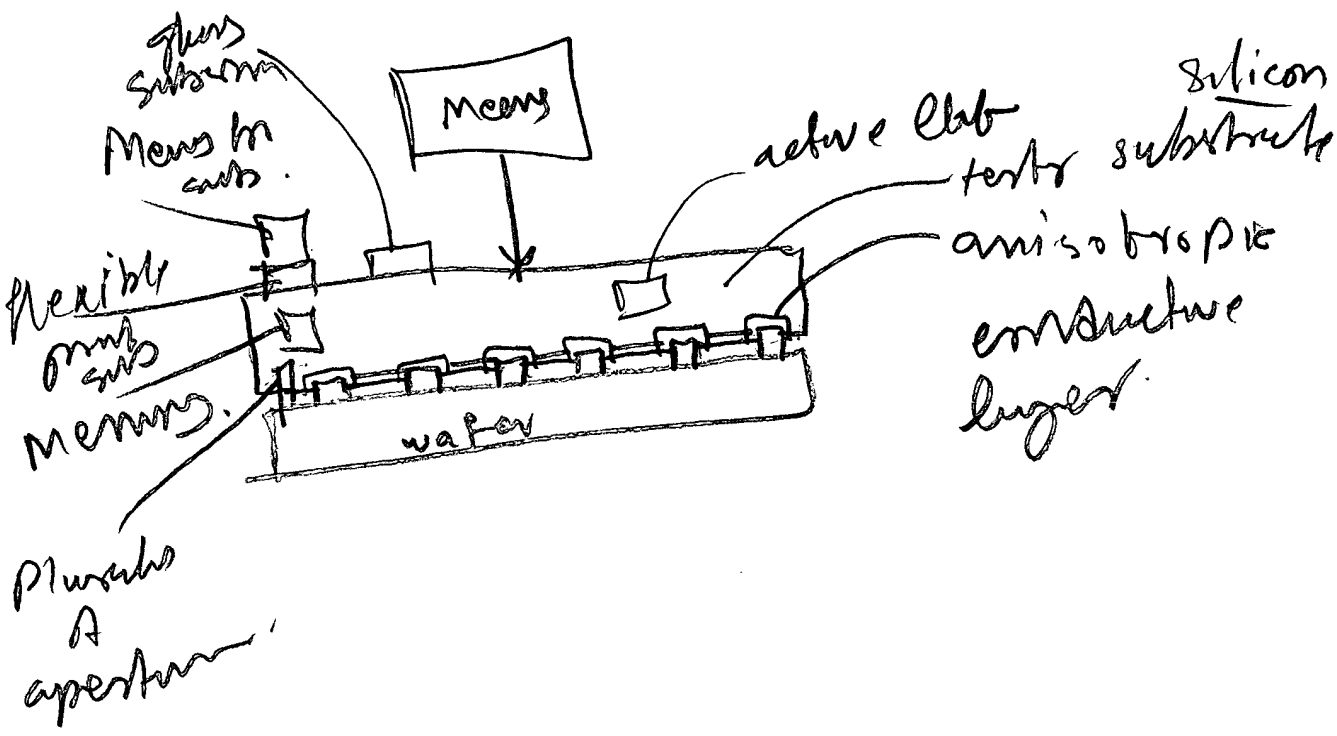
[redacted]



US-PAT-NO: 4385434

DOCUMENT-IDENTIFIER: US 4385434 A

TITLE: Alignment system

---------- KWIC ---------

Detailed Description Text - DETX (24):

Further, although mechanical drives have been illustrated, any other type of drive mechanism may be used. For example, a truss structure 80 may be formed in platen 12c, FIG. 10, having a plurality of beams 82 running in both directions across the bottom of platen 12c separated by holes or bays 84, as shown in FIG. 11. Heat, which may be applied for example by a heat source 86 consisting of a laser beam, may be used to strike selected ones of beams 82 to cause them to expand and deform selected zones on the platen and wafer . The truss structure 80 with bays 84 separating trusses 82 helps to confine the thermal energy paths along the trusses to enable a measure of directionality and control to be exercised over the thermal expansion. Alternatively, heating and cooling may be applied by heaters or Peltier devices applied to or embedded in the truss structure 80c, such as in FIG. 11, wherein heaters 88 are attached directly to trusses 82.

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727		Waf
32	US 5227862 A		USPAT	19930713		Pro
33	US 5220171 A		USPAT	19930615		Waf
34	US 5193347 A		USPAT	19930316		Hel
35	US 4385434 A		USPAT	19830531	10	Ali

Details Text Image HTML

United States Patent [19]

Zehnpfennig et al.

[11] **4,385,434**

[45] **May 31, 1983**

[54] **ALIGNMENT SYSTEM**

[75] Inventors: Theodore F. Zehnpfennig, Wayland; Giuseppe Aurilio, Arlington, both of Mass.

[73] Assignee: Viridyne, Inc., Burlington, Mass.

[21] Appl. No.: 271,786

[22] Filed: Jun. 8, 1981

[51] Int. Cl.³ A61K 27/02; H01L 7/00

[52] U.S. Cl. ..... 29/576 B; 250/492.2

[58] Field of Search ..... 29/577 X, 583, 464, 29/576 B, 576 R; 250/492 A

[56] **References Cited**

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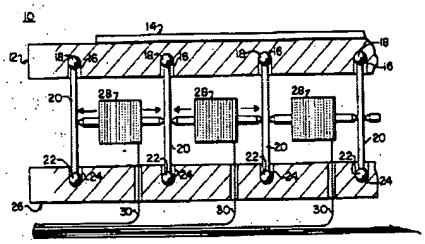
4,322,626 3/1982 Kawashima 250/492.2

Primary Examiner—L. Dewayne Rutledge
Assistant Examiner—David A. Hey
Attorney, Agent, or Firm—Joseph S. Iandiorio

[57] **ABSTRACT**

An alignment system for realigning one portion of an integrated circuit wafer relative to another portion of the same wafer including: a support member for mounting a wafer to be realigned and having a plurality of laterally disposed zones; and means for selectively, laterally deforming the zones of the support member for realigning corresponding portions of a wafer mounted on the support member.

20 Claims, 11 Drawing Figures



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09/673953

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portion of the heat
produced as a result of the X-ray irradiation is diffused over the X-Y plane.
Consequently, a heat flow of a heat flow density of about 1000 W/m.sup.2
impinges on the heat receiving side (Peltier device 104 side) of the heat pipe
105.

Detailed Description Text - DETX (47):

Like the third embodiment, also with the structure of the present embodiment it
is possible to reduce the displacement of the attracting block 101 to be caused
as a result of the exposure operation. Further, since it is sufficient that
the temperature sensor 119 is provided between the wafer and the Peltier device
304, in the present embodiment it may be provided on the heat pipe 305.

Detailed Description Text - DETX (51):

In a portion of the outside surface of a first constituent element 402.sub.1, a
wafer attracting surface 401 is formed. In a portion of the outside surface of
a third constituent element 402.sub.3, a Peltier device 404 is mounted. In the
present embodiment, the bottom face of the wafer attracting surface 401 of the
first constituent element 402.sub.1 provides a heat receiving surface, while

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727		Waf
32	US 5227862 A		USPAT	19930713		Pro
33	US 5220171 A		USPAT	19930615	27	Waf
34	US 5193347 A		USPAT	19930316	12	Hel
35	US 4385434 A		USPAT	19830531	10	Ali

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U.S. Patent June 15, 1993 Sheet 7 of 15 5,220,171

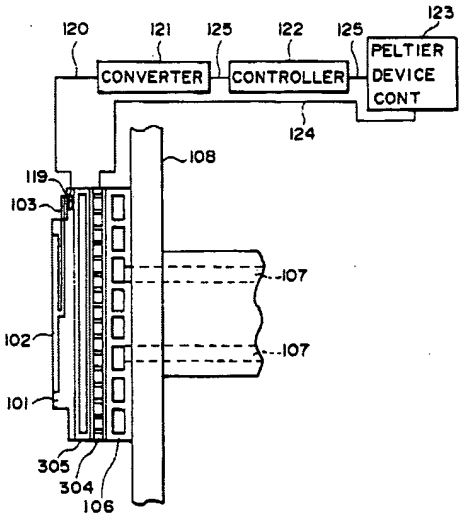

FIG. 7

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EAST Browser - L4: (35) peltier near... | US 5231291 A | Tag: S | Doc: 31/35 | Format: KWIC

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US-PAT-NO: 5231291

DOCUMENT-IDENTIFIER: US 5231291 A

TITLE: Wafer table and exposure apparatus with the same

---------- KWIC ---------

Detailed Description Text - DETX (2):

FIG. 1 schematically illustrates a step-and-repeat type exposure apparatus with a wafer table, according to an embodiment of the present invention. In FIG. 1, denoted at 1 is exposure radiation energy such as light or X-rays, for example, supplied from an exposure radiation source 100; at 2 is a shutter for defining a desired exposure time; at 3 is a mask and at 4 is a wafer. The mask 3 and the wafer 4 are opposed to each other and are substantially parallel to an X-Y plane, with a small gap maintained therebetween. The irradiation of the mask 3 and the wafer 4 with the exposure radiation energy 1 is controlled by opening/closing the shutter 2. Denoted at 5 is a wafer table for holding the wafer 4 thereon. The wafer table is provided with vacuum grooves 6 for holding by vacuum the wafer 4 on its wafer holding surface, a Peltier device 7 effective to transmit the thermal energy produced inside the wafer table by the exposure radiation rays 1 to a constant temperature water side, a flow

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The
31	US 5231291 A		USPAT	19930727	12	Waf
32	US 5227862 A		USPAT	19930713	79	Pro
33	US 5220171 A		USPAT	19930615	27	Waf
34	US 5193347 A		USPAT	19930316	12	Hel
35	US 4385434 A		USPAT	19830531	10	Ali

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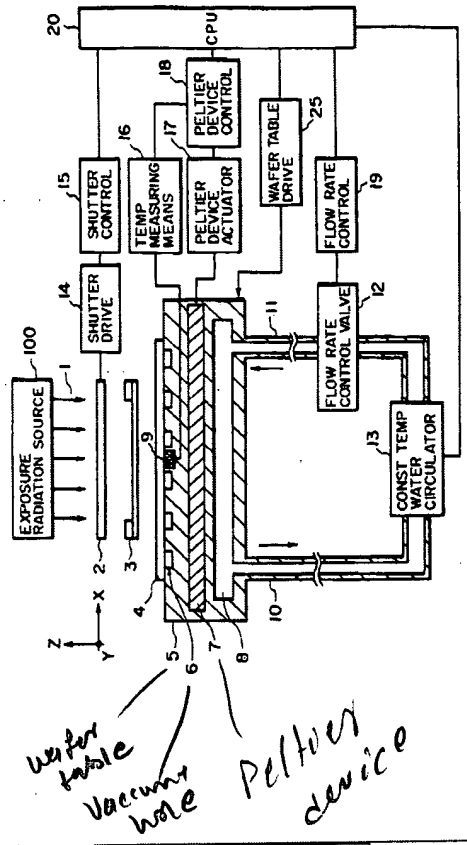

FIG. 1

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US-PAT-NO: 6215545

DOCUMENT-IDENTIFIER: US 6215545 B1

TITLE: Substrate processing apparatus

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Detailed Description Text - DETX (33):

In the example shown in FIG. 7, a wafer W is cooled by water whose temperature
is kept constant, the water being circulated in a circulation path (not shown)
of the cooling table 152. Alternatively, the cooling table 152 may have a
Peltier device so as to cool the wafer W.

	Document ID	Kind Codes	Source	Issue Date	Pages	
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro
26	US RE36242 E		USPAT	19990629	13	Hel
27	US 5894341 A		USPAT	19990413	29	Exp
28	US 5714791 A		USPAT	19980203	9	On-
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The

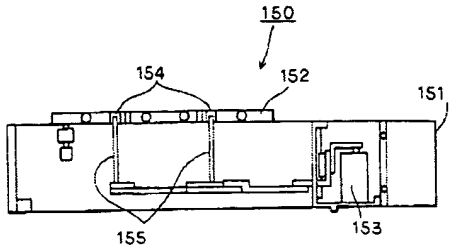

FIG. 7

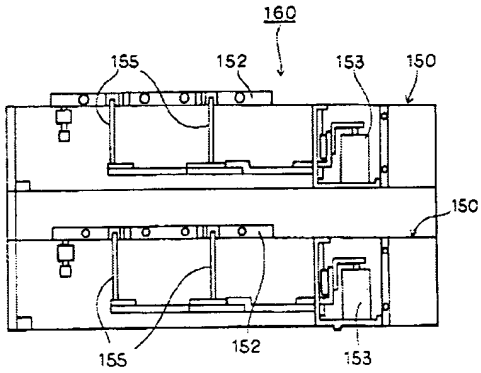

FIG. 8

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US-PAT-NO: 6215545

DOCUMENT-IDENTIFIER: US 6215545 B1

TITLE: Substrate processing apparatus

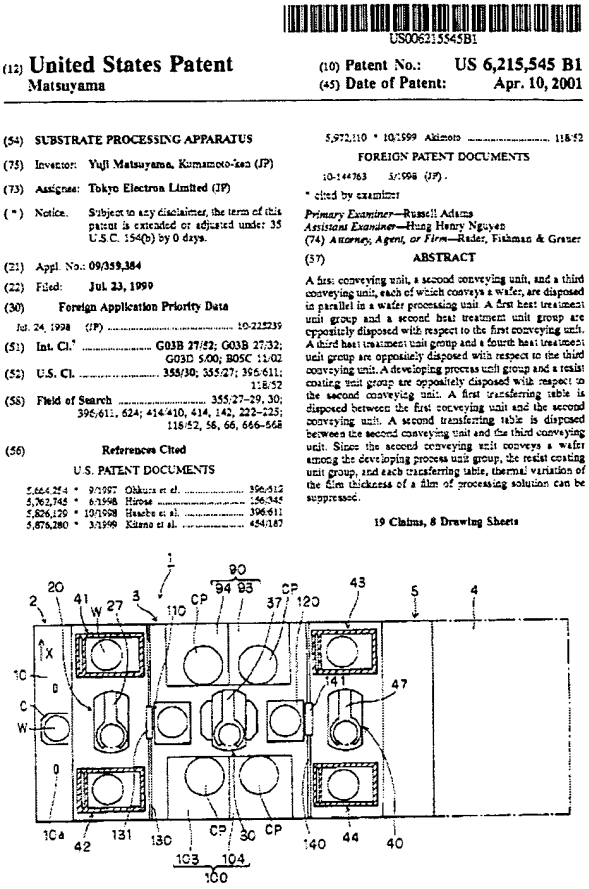
---------- KWIC ---------

Detailed Description Text - DETX (33):

In the example shown in FIG. 7, a wafer W is cooled by water whose temperature
is kept constant, the water being circulated in a circulation path (not shown)
of the cooling table 152. Alternatively, the cooling table 152 may have a
Peltier device so as to cool the wafer W.

Details | Text | Image | HTML | KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro
26	US RE36242 E		USPAT	19990629	13	Hel
27	US 5894341 A		USPAT	19990413	29	Exp
28	US 5714791 A		USPAT	19980203	9	On-
29	US 5401359 A		USPAT	19950328	8	Dry
30	US 5269146 A		USPAT	19931214	7	The



US006215545B1

(12) **United States Patent**
Matsuyama

(10) **Patent No.: US 6,215,545 B1**
(45) **Date of Patent: Apr. 10, 2001**

(54) **SUBSTRATE PROCESSING APPARATUS**

(75) Inventor: **Yuji Matsuyama, Kumamoto-ken (JP)**

(73) Assignee: **Tokyo Electron Limited (JP)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/359,384**

(22) Filed: **Jul. 23, 1999**

(30) **Foreign Application Priority Data**

Jul. 24, 1998 (JP) 10-225239

(51) **Int. Cl.**[7] **G03B 27/52; G03B 27/32; G03D 5/00; B05C 11/02**

(52) **U.S. Cl.** **355/30; 355/27; 396/611; 118/52**

(58) **Field of Search** 355/27-29, 30; 396/611, 624; 414/410, 414, 142, 222-225; 118/52, 56, 66, 666-668

(56) **References Cited**

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5,762,745 * 6/1998 Hirose 156/345
5,826,129 * 10/1998 Hasebe et al. 396/611
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5,972,110 * 10/1999 Akimoto 118/52

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10-144763 5/1998 (JP) .

* cited by examiner

Primary Examiner—Russell Adams
Assistant Examiner—Hung Henry Nguyen
(74) *Attorney, Agent, or Firm*—Rader, Fishman & Grauer

(57) **ABSTRACT**

A first conveying unit, a second conveying unit, and a third conveying unit, each of which conveys a wafer, are disposed in parallel in a wafer processing unit. A first heat treatment unit group and a second heat treatment unit group are oppositely disposed with respect to the first conveying unit. A third heat treatment unit group and a fourth heat treatment unit group are oppositely disposed with respect to the third conveying unit. A developing process unit group and a resist coating unit group are oppositely disposed with respect to the second conveying unit. A first transferring table is disposed between the first conveying unit and the second conveying unit. A second transferring table is disposed between the second conveying unit and the third conveying unit. Since the second conveying unit conveys a wafer among the developing process unit group, the resist coating unit group, and each transferring table, thermal variation of the film thickness of a film of processing solution can be suppressed.

19 Claims, 8 Drawing Sheets

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US-PAT-NO: 6332322

DOCUMENT-IDENTIFIER: US 6332322 B1

TITLE: Electronic device having a thermally isolated element

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Detailed Description Text - DETX (70):

The characteristics of the thin film-shaped Peltier device vary from chip to chip, from wafer to wafer, and from lot to lot. Therefore, the thin film-shaped Peltier device can be used when it is not required to very precisely control the temperature of the functional material 306 at a set value or when the amount of heat generated by the functional material does not vary greatly.

	Document ID	Kind Codes	Source	Issue Date	Pages	
22	US 6332322 B1		USPAT	20011225	21	Ele
23	US 6287435 B1		USPAT	20010911	29	Met
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro
26	US RE36242 E		USPAT	19990629	13	Hel
27	US 5894341 A		USPAT	19990413	29	Exp
28	US 5714791 A		USPAT	19980203	9	On-

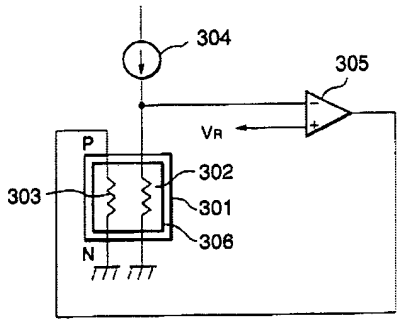

FIG. 4A

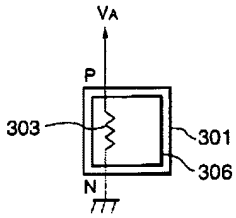

FIG. 4B

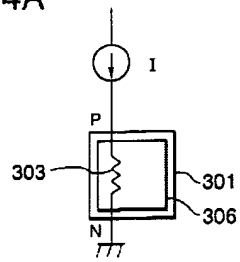

FIG. 4C

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.US-PAT-NO: 6399926

DOCUMENT-IDENTIFIER: US 6399926 B2

TITLE: Heat-treating apparatus capable of high temperature uniformity

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Detailed Description Text - DETX (36):

In the aforementioned embodiments, the description has covered a case where the heat treatment apparatus is to heat the substrate. The present invention is however applicable also to a case of cooling the substrate by using a cooler using an isothermal cooling water jacket or a Peltier device in place of the heater contained in the heat treatment apparatus. While a photomask for semiconductor has been used as an example for description in the aforementioned embodiments, the invention is applicable also to a semiconductor wafer or a liquid crystal panel requiring high-accuracy heat treatment of the substrate.

Details | Text | Image | HTML | KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
21	US 6399926 B2		USPAT	20020604	13	Hea
22	US 6332322 B1		USPAT	20011225	21	Ele
23	US 6287435 B1		USPAT	20010911	29	Met
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro
26	US RE36242 E		USPAT	19990629	13	Hel
27	US 5894341 A		USPAT	19990413	29	Exp

US006399926B2

(12) **United States Patent**
Takano et al.

(10) **Patent No.: US 6,399,926 B2**
(45) **Date of Patent: Jun. 4, 2002**

(54) **HEAT-TREATING APPARATUS CAPABLE OF HIGH TEMPERATURE UNIFORMITY**

(75) Inventors: **Michiro Takano**; **Osamu Kataoka**, both of Kawasaki (JP)

(73) Assignee: **Sigmameltec Ltd.**, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/817,743**

(22) Filed: **Mar. 27, 2001**

(30) **Foreign Application Priority Data**

Apr. 3, 2000 (JP) 2000-137857
Jul. 21, 2000 (JP) 2000-254655

(51) **Int. Cl.**[7] **H05B 1/02**

(52) **U.S. Cl.** 219/497; 219/485; 219/486; 219/121.43; 118/725

(58) **Field of Search** 219/121.43, 121.41, 219/497, 505, 483, 485; 156/345; 118/724, 725; 307/36–41

(56) **References Cited**

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FOREIGN PATENT DOCUMENTS

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JP 7258453 10/1995

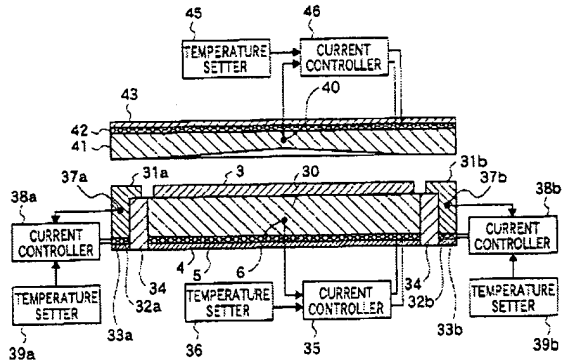
* cited by examiner

Primary Examiner—Mark Paschall
(74) *Attorney, Agent, or Firm*—Stevens, Davis, Miller & Mosher, LLP

(57) **ABSTRACT**

A heat treatment apparatus permits manufacture of a high-accuracy resist pattern by reducing a temperature difference within a substrate surface in the transition state of heating or cooling the substrate and the steady state. The heat treatment apparatus includes a thermal plate having a main surface containing a first area on which the substrate is to be placed and a second area surrounding the first area, heat capacity per unit area in the second area of the main surface being smaller than heat capacity per unit area in the first area of the main surface, and a temperature control element for controlling temperature of the thermal plate in accordance with supplied current.

24 Claims, 7 Drawing Sheets



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DOCUMENT-IDENTIFIER: US 20020158328 A1

TITLE: Ceramic substrate for semiconductor fabricating device

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Brief Description of Drawings - Table CWU - DRTL (1):

1 Explanation of Symbols 1, 11, 63 ceramic substrate 2, 22, 32a, 32b chuck positive electrostatic layer 3, 23, 33a, 33b chuck negative electrostatic layer 2a, 3a semicircular arc part 2b, 3b combteeth-shaped part 4 ceramic dielectric film 5, 12, 25, 61 resistance heating element 6, 13, 18 external terminal 7 metal wire 8 Peltier device 9 silicon wafer 10 ceramic heater 14 bottomed hole 15 through hole 16, 17, 19 conductor-filled through hole 20, 30, 101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet 45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground electrode 66a non-electrode formied area 67 groove 68 suction hole 501 wafer prober

	Document ID	Kind Codes	Source	Issue Date	Pages	
1	US 20020158328		US-PGPUB	20021031	28	Ceram
2	US 20010002918		US-PGPUB	20010607	15	Surfa
3	US 6507006 B1		USPAT	20030114	21	Ceran
4	US 6464393 B2		USPAT	20021015	16	Surfa

US 20020158328A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0158328 A1

Hiramatsu et al. (43) Pub. Date: Oct. 31, 2002

(54) CERAMIC SUBSTRATE FOR SEMICONDUCTOR FABRICATING DEVICE

(76) Inventors: Yasuji Hiramatsu, Gifu (JP); Yasutaka Ito, Gifu (JP)

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ARLINGTON, VA 22202 (US)

(21) Appl. No.: 09/926,800

(22) PCT Filed: Apr. 18, 2001

(86) PCT No.: PCT/JP01/03299

(30) Foreign Application Priority Data

Apr. 24, 2000 (JP) 2000-121936

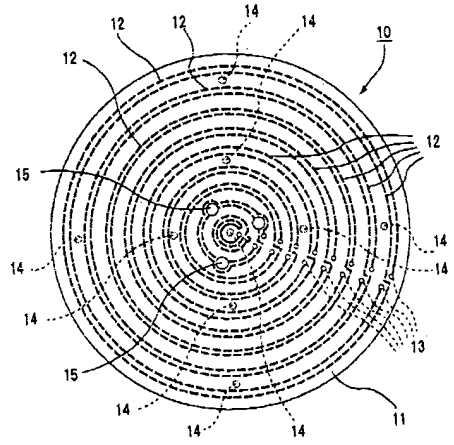
Publication Classification

(51) Int. Cl.[7] H01L 23/053

(52) U.S. Cl. 257/700

(57) ABSTRACT

The objective of the invention is to provide a ceramic substrate: wherein even if rapid temperature rising or rapid temperature falling is conducted, no problem of cracking or warp of the ceramic substrate occurs; wherein, in case that the ceramic substrate is a ceramic substrate constituting an electrostatic chuck, local dispersion of chuck power is eliminated, in case that the ceramic substrate is a ceramic substrate constituting a hot plate, local dispersion of temperature of a wafer treating face is eliminated, in case that the ceramic substrate is a ceramic substrate constituting a wafer prober, dispersion of applied voltage of a guard electrode or a ground electrode is eliminated and a stray capacitor or noise can be eliminated. The ceramic substrate of the present invention is a ceramic substrate provided with a conductor layer on the surface of the ceramic substrate or inside the ceramic substrate, wherein the ratio (t_2/t_1) of the average thickness of the conductor layer (t_2) to the average thickness of the ceramic substrate (t_1) is less than 0.1 and; a dispersion of the thickness of the conductor layer to the average thickness of the conductor layer is in a range of −70 to +150%.



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EAST Browser - L2: (4) peltier same... | US 20010002918 | Tag: S | Doc: 2/4 | "Full" 1/15 (Total images 15)

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DOCUMENT-IDENTIFIER: US 20010002918 A1

TITLE: Surface temperature sensor head

---------- KWIC ---------

Summary of Invention Paragraph - BSTX (22):

[0020] This improvement contrives to reduce the temperature fluctuation induced by the touch of the probe needles by maintaining the probe at the same temperature as the wafer . For the purpose, this improvement provides the probe with a Peltier device and a temperature sensor. The Peltier device can heat or cool the probe by alternating the directions of current flow. The temperature sensor is a thermocouple. The tip of the thermocouple is buried into the probe for sensing exact temperature of the probe . The reason why the tip is buried into the probe is that exact temperature can be measured by reducing the heat resistance between the tip and the probe .

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
1	US 20020158328		US-PGPUB	20021031	28	Ceran
2	US 20010002918		US-PGPUB	20010607	15	Surfa
3	US 6507006 B1		USPAT	20030114	21	Ceran
4	US 6464393 B2		USPAT	20021015	16	Surfa

Details Text Image HTML

US 20010002918A1

(19) **United States**

(12) **Patent Application Publication** (10) Pub. No.: US 2001/0002918 A1

Tatoh (43) Pub. Date: Jun. 7, 2001

(54) SURFACE TEMPERATURE SENSOR HEAD

(75) Inventor: Nobuyoshi Tatoh, Hyogo (JP)

Correspondence Address:
McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096 (US)

(73) Assignee: Sumitomo Electric Industries, Ltd.

(21) Appl. No.: 09/725,502

(22) Filed: Nov. 30, 2000

(30) Foreign Application Priority Data

Dec. 3, 1999 (JP) 344569/1999

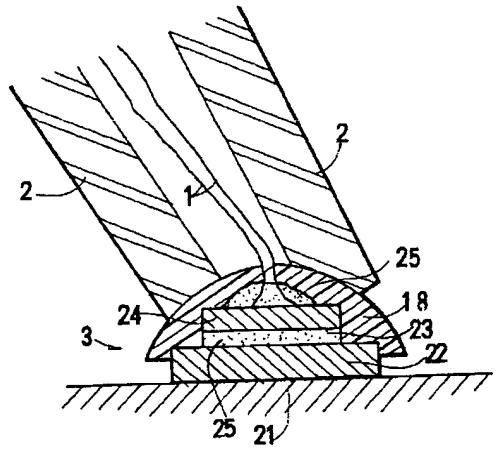
Publication Classification

(51) Int. Cl.[7] H01L 35/02; G01K 7/04

(52) U.S. Cl. 374/179; 136/230

(57) ABSTRACT

A surface temperature sensor head including a first layer made of a material of a heat conductivity higher than 100 W/mK, a second layer having a crossing tips of a thermocouple and a brazing material and a third layer made of a material of a heat conductivity higher than 100 W/mK, the brazing material unifying the crossing tips, the first layer and the third layer. The sensor head enables a temperature probes to measure temperatures of an object non-destructively with high spatial resolution.



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EAST Browser - L2: (4) peltier same... | US 6507006 | Tag: S | Doc: 3/4 | "Full" 1/21 (Total images 21)

File Edit View Tools Window Help

Courier New 12

US-PAT-NO: 6507006

DOCUMENT-IDENTIFIER: US 6507006 B1

TITLE: Ceramic substrate and process for producing the same

---------- KWIC ---------

Detailed Description Text - DETX (1):

EXPLANATION OF SYMBOLS 1, 11, 63 ceramic substrate 2, 22, 32a, 32b chuck
positive electrode electrostatic layer 3, 23, 33a, 33b chuck negative electrode
electrostatic layer 2a, 3a semicircular part 2b, 3b comb-teeth-shaped part 4
ceramic dielectric film 5, 12, 25, 61 resistance heating element 6, 13, 18
external terminal 7 metal line 8 Peltier device 9 silicon wafer 10 ceramic
heater 14 bottomed hole 15 through hole 16, 17, 18 plated through hole 20, 30,
101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind
hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet
45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground
electrode 66a non-electrode forming area 67 groove 68 suction hole 501 wafer
prober

Details Text Image HTML KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
1	US 20020158328		US-PGPUB	20021031	28	Ceran
2	US 20010002918		US-PGPUB	20010607	15	Surfa
3	US 6507006 B1		USPAT	20030114	21	Ceran
4	US 6464393 B2		USPAT	20021015	16	Surfa

Details Text Image HTML

US006507006B1

(12) **United States Patent**
Hiramatsu et al.

(10) **Patent No.: US 6,507,006 B1**
(45) **Date of Patent: Jan. 14, 2003**

(54) **CERAMIC SUBSTRATE AND PROCESS FOR PRODUCING THE SAME**

(75) Inventors: Yasuji Hiramatsu, Gifu (JP); Yasutaka Ito, Gifu (JP)

(73) Assignee: Ibiden Co., Ltd., Ogaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/869,594

(22) PCT Filed: May 15, 2000

(86) PCT No.: PCT/JP00/03080

§ 371 (c)(1),
(2), (4) Date: Aug. 9, 2001

(87) PCT Pub. No.: WO01/63972

PCT Pub. Date: Aug. 30, 2001

(30) **Foreign Application Priority Data**

Feb. 25, 2000 (JP) 2000-049482

(51) Int. Cl.[7] H05B 3/68

(52) U.S. Cl. 219/444.1

(58) Field of Search 219/444.1, 460.1, 219/461.1, 465.1, 466.1, 467.1, 468.1, 543, 544, 546, 547, 548; 338/307, 308, 314; 118/724, 725

(56) **References Cited**

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4,443,691 A * 4/1984 Sater 219/203
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5,072,236 A * 12/1991 Tabuchi et al. 219/543
6,080,970 A * 6/2000 Yoshida et al. 118/725
6,133,557 A * 10/2000 Kawasabe et al. 219/544

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JP	8-273814	10/1996
JP	9-180867	7/1997
JP	2000-12194	1/2000

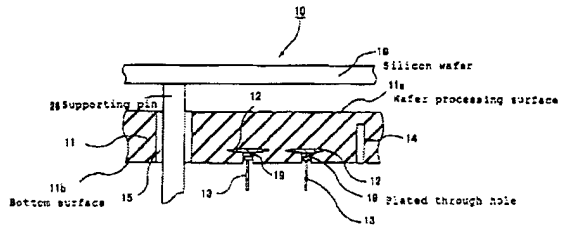
* cited by examiner

Primary Examiner—Sang Paik
(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) **ABSTRACT**

An object of the present invention is to provide a ceramic substrate that is superior in heat uniformity and thermal shock resistance, and has a large chuck power in the case that the ceramic substrate is made to be an electrostatic chuck. The ceramic substrate of the present invention is a ceramic substrate comprising a conductor layer formed therein, characterized in that a section of the edge of the conductor layer is in a peaked shape.

18 Claims, 8 Drawing Sheets



One inventor is common same assignee

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File Edit View Tools Window Help

Courier New 12

US-PAT-NO: 6464393

DOCUMENT-IDENTIFIER: US 6464393 B2

TITLE: Surface temperature sensor head

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Brief Summary Text - BSTX (22):

This improvement contrives to reduce the temperature fluctuation induced by the touch of the probe needles by maintaining the probe at the same temperature as the wafer . For the purpose, this improvement provides the probe with a Peltier device and a temperature sensor. The Peltier device can heat or cool the probe by alternating the directions of current flow. The temperature sensor is a thermocouple. The tip of the thermocouple is buried into the probe for sensing exact temperature of the probe . The reason why the tip is buried into the probe is that exact temperature can be measured by reducing the heat resistance between the tip and the probe .

Details | Text | Image | HTML | KWIC

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2	US 20010002918		US-PGPUB	20010607	15	Surfa
3	US 6507006 B1		USPAT	20030114	21	Ceran
4	US 6464393 B2		USPAT	20021015	16	Surfa

Details | Text | Image | HTML

US006464393B2

(12) **United States Patent**
Tatoh

(10) **Patent No.: US 6,464,393 B2**
(45) **Date of Patent: Oct. 15, 2002**

(54) **SURFACE TEMPERATURE SENSOR HEAD**

(75) Inventor: **Nobuyoshi Tatoh**, Hyogo (JP)

(73) Assignee: **Sumitomo Electric Industries, Ltd.**, Osaka (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 23 days.

(21) Appl. No.: **09/725,502**

(22) Filed: **Nov. 30, 2000**

(65) **Prior Publication Data**

US 2001/0002918 A1 Jun. 7, 2001

(30) **Foreign Application Priority Data**

Dec. 3, 1999 (JP) 11-344569

(51) Int. Cl.[7] G01K 7/00

(52) U.S. Cl. 374/179; 136/233

(58) Field of Search 374/120, 179; 136/232, 233, 236.1

(56) **References Cited**

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JP	05118925	A *	5/1993	374/120
JP	7-74218		3/1995	
JP	11-125566		5/1999	

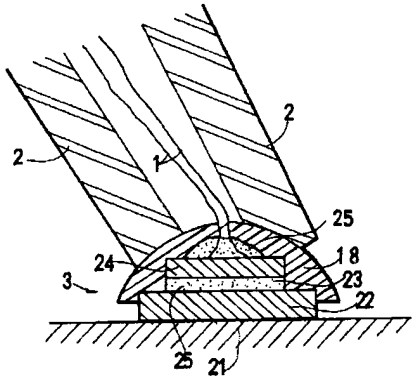
* cited by examiner

Primary Examiner—Diego Gutierrez
Assistant Examiner—Mirellys Jagan
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A surface temperature sensor head including a first layer made of a material of a heat conductivity higher than 100 W/mK, a second layer having a crossing tips of a thermocouple and a brazing material and a third layer made of a material of a heat conductivity higher than 100 W/mK, the brazing material unifying the crossing tips, the first layer and the third layer. The sensor head enables a temperature probe to measure temperatures of an object non-destructively with high spatial resolution.

20 Claims, 7 Drawing Sheets



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US-PAT-NO: 6507006

DOCUMENT-IDENTIFIER: US 6507006 B1

TITLE: Ceramic substrate and process for producing the same

---------- KWIC ---------

Detailed Description Text - DETX (1):

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101, 201, 301, 401 electrostatic chuck 25a metal covering layer 35, 36 blind
hole 41 supporting case 42 coolant outlet 43 inhalation duct 44 coolant inlet
45 heat insulator 62 chuck top conductor layer 65 guard electrode 66 ground
electrode 66a non-electrode forming area 67 groove 68 suction hole 501 wafer
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19	US 6507006 B1		USPAT	20030114	21	Cer
20	US 6464393 B2		USPAT	20021015	16	Sur
21	US 6399926 B2		USPAT	20020604	13	Hea
22	US 6332322 B1		USPAT	20011225	21	Ele
23	US 6287435 B1		USPAT	20010911	29	Met
24	US 6215545 B1		USPAT	20010410	17	Sub
25	US 6094268 A		USPAT	20000725	74	Pro

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US006507006B1

(12) **United States Patent**
Hiramatsu et al.

(10) **Patent No.: US 6,507,006 B1**
(45) **Date of Patent: Jan. 14, 2003**

(54) **CERAMIC SUBSTRATE AND PROCESS FOR PRODUCING THE SAME**

(75) Inventors: Yasuji Hiramatsu, Gifu (JP); Yasutaka Ito, Gifu (JP)

(73) Assignee: Ibiden Co., Ltd., Ogaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/869,594

(22) PCT Filed: May 15, 2000

(86) PCT No.: PCT/JP00/03080

§ 371 (c)(1),
(2), (4) Date: Aug. 9, 2001

(87) PCT Pub. No.: WO01/63972

PCT Pub. Date: Aug. 30, 2001

(30) **Foreign Application Priority Data**

Feb. 25, 2000 (JP) 2000-046482

(51) Int. Cl.[7] H05B 3/68

(52) U.S. Cl. 219/444.1

(58) Field of Search 219/444.1, 460.1, 219/461.1, 465.1, 465.1, 467.1, 468.1, 543, 544, 546, 547, 548; 338/307, 308, 314; 118/724, 725

(56) **References Cited**

U.S. PATENT DOCUMENTS

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5,072,236 A * 12/1991 Tamura et al. 219/543
6,080,976 A * 6/2000 Yoshida et al. 118/725
6,133,557 A * 10/2000 Kawanabe et al. 219/544

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JP 6-5974 2/1994
JP 8-273814 10/1995
JP 9-180857 7/1997
JP 2000-12194 1/2000

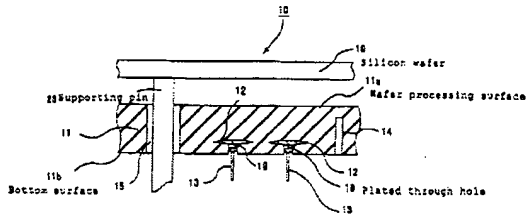
* cited by examiner

Primary Examiner—Sang Paik
(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) **ABSTRACT**

An object of the present invention is to provide a ceramic substrate that is superior in heat uniformity and thermal shock resistance, and has a large chuck power in the case that the ceramic substrate is made to be an electrostatic chuck. The ceramic substrate of the present invention is a ceramic substrate comprising a conductor layer formed therein, characterized in that a section of the edge of the conductor layer is in a peaked shape.

18 Claims, 8 Drawing Sheets



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US-PAT-NO: 3037064

DOCUMENT-IDENTIFIER: US 3037064 A

TITLE: Method and materials for obtaining low resistance bonds to thermoelectric bodies

---------- KWIC ---------

OCR Scanned Text - LPAR (2):

r T 3,037,064 U iLiLlted States Patent Office Patented May 29, 1962 2 the amount of Peltier cooling by as much as 25%. For the effect of contact resistance on maximum cooling ob- tained in Peltier devices, see FIG. 5 of chapter 8, "Evaluatio n and Properties of Materials for Thermoele ctric Ap- plications," by F. D. Rosi and E. G. Ramberg, in "Thermoel ectricity," edited by P. H. Egli, John Wiley and Sons, Inc., New York, 1960. It is therefor e an object of the instant invention to provide improve d methods and material s for making low re- 10 sistance electrical contacts to thermoelec tric circuit members. Another object of the invention is to provide improve d methods and material s for obtaining res tance, mechani cary strong electrica l connecti ons to thermoel ectric 15 component s. A further object of

Details | Text | Image | HTML | KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
21	US 3220198 A		USOCR	19651130	7	The
22	US 3192727 A		USOCR	19650706	5	Iso
23	US 3181304 A		USOCR	19650504	3	Pel
24	US 3075031 A		USOCR	19630122	6	Lea
25	US 3037065 A		USOCR	19620529	5	Met
26	US 3037064 A		USOCR	19620529	4	Met

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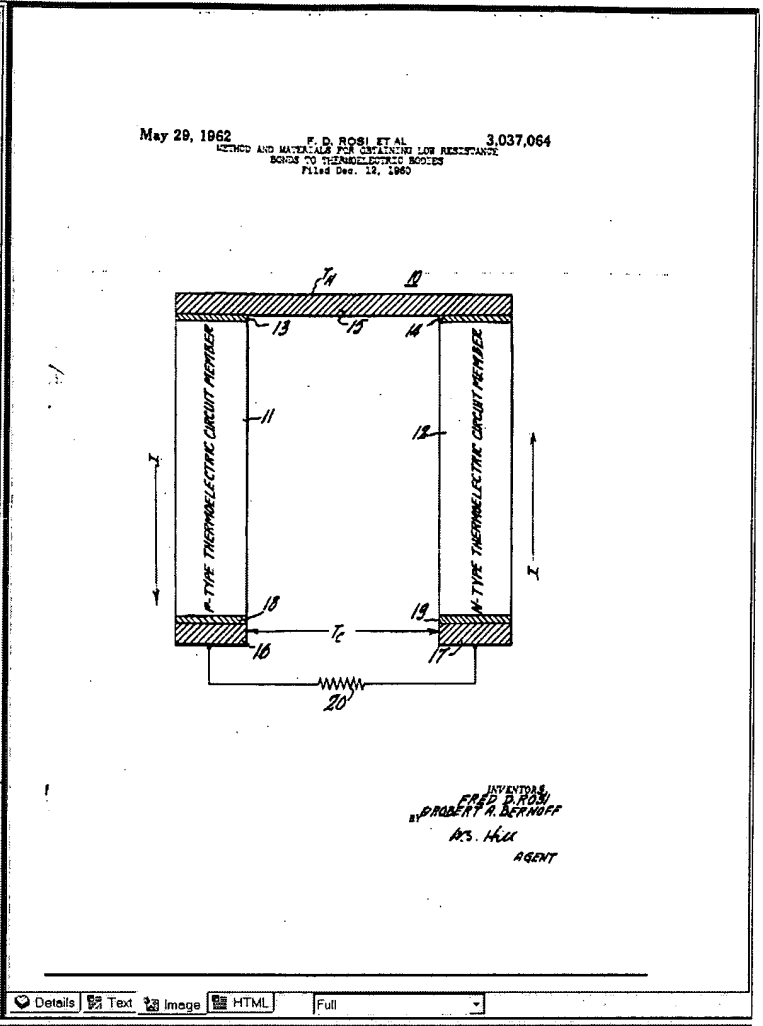

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09/873953

thermoelectric members, or the auxiliary components, or the@ electrical
contarts to the two members, will reduce the efficiency of the device.
Thermoelectric @devires which utilize electrical energy for environmental
cooling and refrigeration by means of the Peltier effect also include two
thermoelectrically com- Patented May 29, 1962 2 30 amperes at 0.1 volt.
Accordingly, if any high resistanc@- contacts are present, considerable Joulean
heat will be!dissipated, and the efficiency of the device will be decreased.
The presence of high resistance contacts on the thermoelectric bodies has been
la serious problem in the falbrication of both Seebeck and Peltier
thermoelectric devices. High resistance contacts can reduce the cooling
produced by Peltier devices as much as 40% below the theoretical maximum value.
A contact resistance of only 10 1/4 of the sum of the resistance of the two
thermoelements in a Peltier device can reduce the amount of Peltier cooling by
as muchas 25%. For a more complete discussion of the effect of contact
resistance on maximum cooling obtained in Peltier devices, see chapter 8,
"Evaluation and 15 Properties of Materials for Thermoelectric AppEcations," by
F. D. Rosi and E. G. Ramberg, in "Thermoelectricity," edited by P. H. Egli,
John Wiley :and Sons, Inc., New York, 1960. It is therefore an object of the
instant invention to pro- 20 vide improved thermoelectric devices. Another
object of t@he invention is to provide improved methods for

Details | Text | Image | HTML | KWIC

	Document ID	Kind Codes	Source	Issue Date	Pages	
20	US 3226804 A		USOCR	19660104	3	Metl
21	US 3220198 A		USOCR	19651130	7	The
22	US 3192727 A		USOCR	19650706	5	Iso
23	US 3181304 A		USOCR	19650504	3	Pel
24	US 3075031 A		USOCR	19630122	6	Lea
25	US 3037065 A		USOCR	19620529	5	Met
26	US 3037064 A		USOCR	19620529	4	Metl

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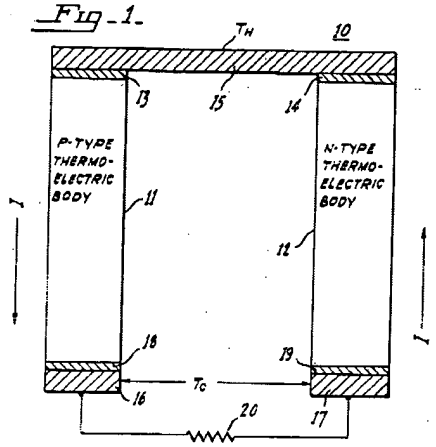
May 29, 1962 E. F. HOCKINGS ETAL 3,037,065
METHOD AND MATERIALS FOR THERMOELECTRIC BODIES
Filed May 12, 1961

Fig. 1.



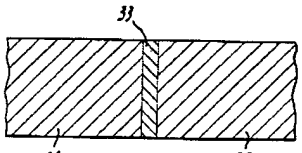


Fig. 2.

INVENTORS
ERIC F. HOCKINGS &
BY WALTER L. MULARE
W. S. Hill
AGENT

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